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Synchronous Up / Down Counter in CMOS Technology with High-Speed Local Clock Generation Utilizing Gate Driver Logic

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Abstract*— This study introduces the design and construction of a synchronous counter in CMOS technology, focusing on the generation of a high-speed local clock through the application of gate driver logic. The counter is designed to offer both upward and downward counting capabilities, ensuring efficient and dependable counting processes. By employing gate driver logic for flip-flops, the counter achieves superior speed, which significantly enhances the overall performance. The abstract details the design approach, highlighting the integration of high-speed local clock generation. This investigation provides significant contributions to the advancement of synchronous counters in CMOS technology, proposing a novel method for achieving rapid counting operations.

Keywords: Synchronous Counter, CMOS, Gate Driver Logic.

I. INTRODUCTION

In the realm of modern digital systems, counters are indispensable for a wide range of applications, including frequency synthesis, signal processing, and data communication. The need for counters that offer high-speed performance and the ability to count both upwards and downwards has grown significantly. This study addresses this need by suggesting a design that merges the advantages of CMOS technology with innovative gate driver logic to achieve synchronous operation and high-speed local clock generation. The incorporation of CMOS technology in the counter design ensures minimal power consumption, making the proposed counter ideal for applications that prioritize energy efficiency. Furthermore, the application of gate driver logic enhances the speed of local clock generation, facilitating quicker counting operations. This introduction lays the groundwork for a detailed examination of the proposed counter's architecture, design considerations, and its potential to advance digital circuitry.

The subsequent sections will conduct an in-depth analysis of the current literature concerning counters, the importance of synchronous up/down counters, the contribution of CMOS technology, and the novel approach of integrating high-speed local clock generation via gate driver logic into the counter design. This investigation aims to offer a thorough grasp of the research background and underscore the necessity for the proposed counter structure.

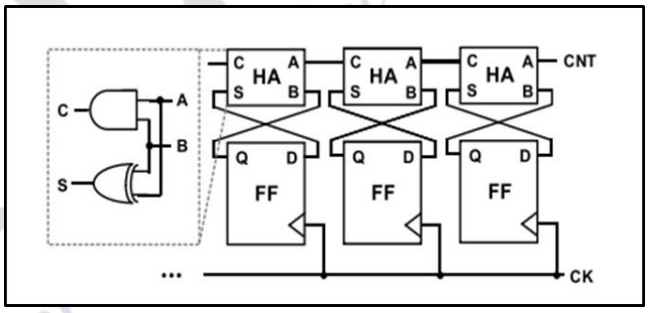

Fig.1: Synchronous Counter [18]

A synchronous counter design typically employs half-adders and D flip-flops (DFFs), as depicted in Figure 1 [18]. This configuration provides simplicity and efficiency in terms of transistor count. Nonetheless, despite its straightforward structure and relatively low transistor requirement, this counter configuration has inherent limitations that restrict its applicability for applications requiring high-speed and low-power characteristics. A significant drawback of the described synchronous counter is its performance constraints, particularly in terms of speed and power efficiency.

II. RELATED WORK

The synchronous counter design that incorporates a data-transition look-ahead (DL) circuit, as suggested by Nogawa and Ohtomo[25], shows significant limitations despite its power-saving advantages. The main benefit is the reduction in dynamic power consumption by eliminating unnecessary internal clock transitions when input and output

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data are identical, leading to a total power reduction of about 27%. However, this method introduces stability issues related to dynamic nodes, which could potentially affect the counter's reliable operation. Moreover, the addition of extra components like pulse generators to implement the DL circuit increases the device count, reducing the simplicity and efficiency typically associated with synchronous counters. These drawbacks underscore the need for further research and innovation in synchronous counter designs to address stability issues and minimize the impact of additional circuitry on overall performance.

Kim et al.'s [27] proposed low-power CMOS synchronous counter, which integrates clock gating into the carry propagation circuit, provides significant power reduction and area efficiency by eliminating unnecessary transitions. However, this design has notable drawbacks. As the counter bit count increases, the delay in carry propagation significantly rises, affecting overall performance. Moreover, the design does not support down-counting operations, restricting its versatility. Additionally, the flip-flops used to store counter bits are not optimized, leading to increased power consumption and area usage. While this approach shows potential in specific applications, these limitations highlight the need for further research and innovation in synchronous counter designs to address scalability, bidirectionality, and optimization challenges for a more comprehensive and versatile counter design.

Harris and Weste [18] underscore the straightforwardness and transistor efficiency of synchronous counters, making them appropriate for a wide range of applications. However, challenges emerge when addressing high-speed and low-power needs. The performance of synchronous counters is hindered by extended propagation delays along ripple carry chain routes, which become increasingly problematic as the counter bit count grows. The ripple effect intensifies, negatively impacting speed. Moreover, the counter shows excessively high switching power consumption, due to numerous redundant transitions, particularly in higher-weight counter bits. These shortcomings highlight the counter's inability to meet the demands of high-speed and low-power applications, indicating a need for more sophisticated design approaches.

Bae et al. [19] present a novel method for high-speed counters using a linear feedback shift register (LFSR) as a state generator, which is particularly advantageous for applications requiring wide bit widths. Despite its benefits in enhancing counting speed, the LFSR implementation has its limitations. The main drawbacks include taking up a significant amount of area and consuming excessive redundant power during counting operations. These challenges underscore the difficulties in achieving both speed and efficiency in counters with wide bit widths, indicating a need for further innovations to address these issues.

Aloisi and Mita [21] suggest a clock-gating technique for linear-feedback shift registers (LFSRs) to decrease overall power consumption by removing redundant transitions during idle computation periods. Despite its potential to enhance power efficiency, this method has its limitations. A significant drawback is the increase in device count due to the need for additional transistors to implement the clock-gating logic. While effective in reducing power consumption, this limitation underscores the trade-off between power efficiency and increased device complexity, highlighting the necessity for optimization strategies in clock-gating designs for LFSRs.

III. TRADITIONAL COUNTER

To enhance counting speed, we employ a high-speed carry selection technique, opting for a single Manchester carry chain to minimize power and area overheads. This counter is versatile, supporting both up-counting and down-counting operations.

The counter architecture, depicted in Fig. 2, is meticulously segmented into circuit blocks, each responsible for managing four counter bits. These segments are equipped with specialized components to facilitate efficient counting operations. The segment with the least significant bit (LSB) incorporates a local clock generator (LCG) that produces pulsed local clocks (LC0-LC3) for the bits with lower weight. In contrast, other parts of the system utilize local clock pre-evaluators (LCPEs) and local clock selectors (LCSs) to manage bits with higher weight. The LCG within the LSB segment is designed to create customized pulsed local clocks, whereas LCPEs are designed to prepare for incoming carry inputs from lower-weight bit positions, thereby efficiently handling bits with higher weight.

Local clock selectors (LCSs), embedded within each segment, are tasked with the creation of valid local clocks (LC4-LC(n-1)), where n signifies the total count of counter bits, specifically for the higher-weight counter bits

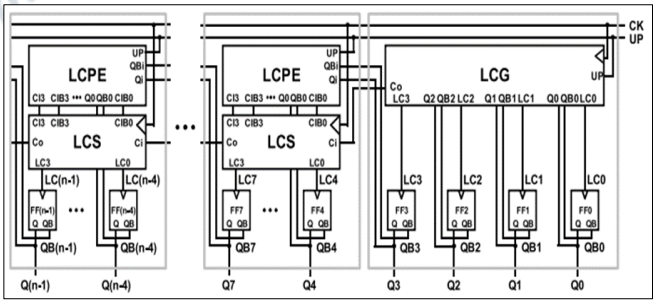

Fig.2: overall block diagram of the Traditional synchronous up/down counter.

Redundant Transition-Free Up/Down Counting:

In a binary counter, the switching activity is maximal (100%) for the least significant bit (LSB) and decreases by half for each subsequent higher-weight bit. Traditional synchronous counters update all bits at each clock edge, irrespective of state changes, leading to redundant transitions and unnecessary power consumption, particularly for

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higher-weight bits. To mitigate this, identifying the transition conditions for each counter bit is crucial for eliminating redundant transitions and optimizing power efficiency.

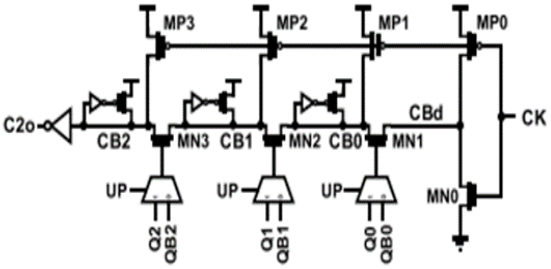

Fig.3: Structure of LCG

The LSB four counter bits employ a Local Clock Generator (LCG) structure in fig.3, akin to the Manchester carry chain but with added multiplexers to facilitate both up and down counting based on specific transition conditions. The enhanced local clock generator (LCG) aids in rapid carry propagation from the least significant bit (LSB) to the most significant bit (MSB), producing pulsed local clocks. Multiplexers enable the choice of counter bit polarities based on the counting direction, and a streamlined keeper circuit minimizes the device count for improved reliability in static operation. During the down-counting process, carry bits (CBd, CB0-CB2) function solely as local clocks when all lower counter bits are at zero. Conversely, during up-counting, they become active when all lower bits are at one, ensuring effective state updates for the flip-flops.

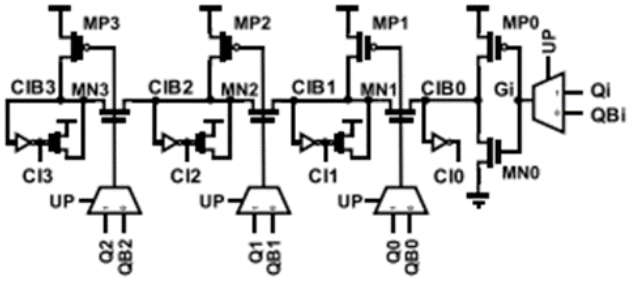

Fig.4: Structure of LCPE.

In the depicted LCPE, akin to the LCG, multiplexers are utilized to support both ascending and descending counting operations. During ascending counting, if the highest-weight counter bit from the preceding segment is inactive, the counter bits within a segment remain static.

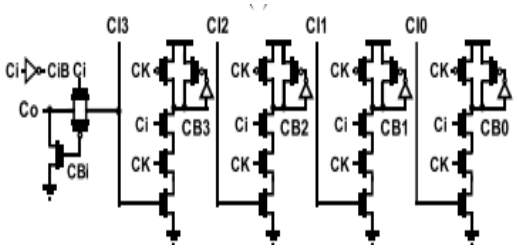

Fig.5: Structure of LCS

In the LCS stage depicted in figure 5, there might be a significant delay between the initiation of the input carry Ci and its subsequent elevation following the activation of Gi. During this interval, keepers sustain the high voltages of CB0-CB3. Upon Ci transitioning to a high state, indicating that all lower-weight counter bits are at their maximum, CB0-CB3 can be reduced based on the current values of the counter bits. This enables the associated flip-flops to refresh their states at the subsequent rising edges of the local clocks.

Compact Toggle Flip-Flop Design

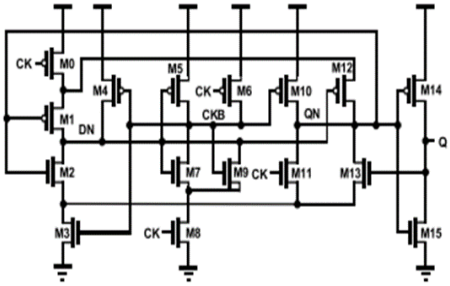

Fig.6: Topology of Toggle Flip-flop

Given a low output, during the low phase of CK (top left cell), M6 increases CKB. This leads to the high value of QN or the input causing DN to be lowered by M2 and M3. As CK ascends (bottom left cell), M11's activation quickly lowers QN, resulting in Q swiftly transitioning to a high state. Upon CK's reversion to a low phase (top right cell), the low value of QN allows DN to ascend through M0 and M1, reestablishing CKB to a high state. As CK ascends once more (bottom right cell), CKB changes to a low state due to the combined influence of M7 and M8, supported by the weaker sizing of keeper M9. This action lifts QN, causing Q to descend to a low state.

IV. PROPOSED STRUCTURE

In this Section, the methodology of Power gating and its significance is discussed elaborately. The design of compact toggle flip-flop from the conventional design is modified with light mode power gating. Here, the modified structure of flip-flop also will be analyzed and presented a novel counter design with this modified flip-flop architecture.

Power Gating:

The utilization of a diode-connected PMOS bias transistor for regulating the virtual ground is suggested.

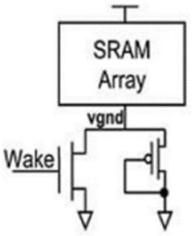

Fig.7: Block diagram of Power Gating [Light sleep mode]

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The PMOS transistor functions akin to a diode by linking its source and gate terminals together, a method known as the self-biasing technique, regulating the virtual ground. Nonetheless, employing the self-biasing technique in nanometer-scale technology encounters several challenges. Firstly, integrating an additional self-biasing transistor (SBT) necessitates extra area, approximately 5%. Secondly, these approaches often inadequately address the modified source voltage mechanism. Lastly, elevating the virtual ground voltage poses significant issues such as negative bias temperature instability (NBTI) or positive bias temperature instability (PBTI).

Modified Flip-Flop architecture:

As per the block diagram of power gating is mentioned in above, the flip-flop architecture is added in the block of the SRAM array. The flip-flop design is of T FF and the structure maintained is of D-FF. We are aware of the methodology to design a T-Flip flop using D-FF. For this, we need to connect Qbar output as D input to work as Toggle FF.

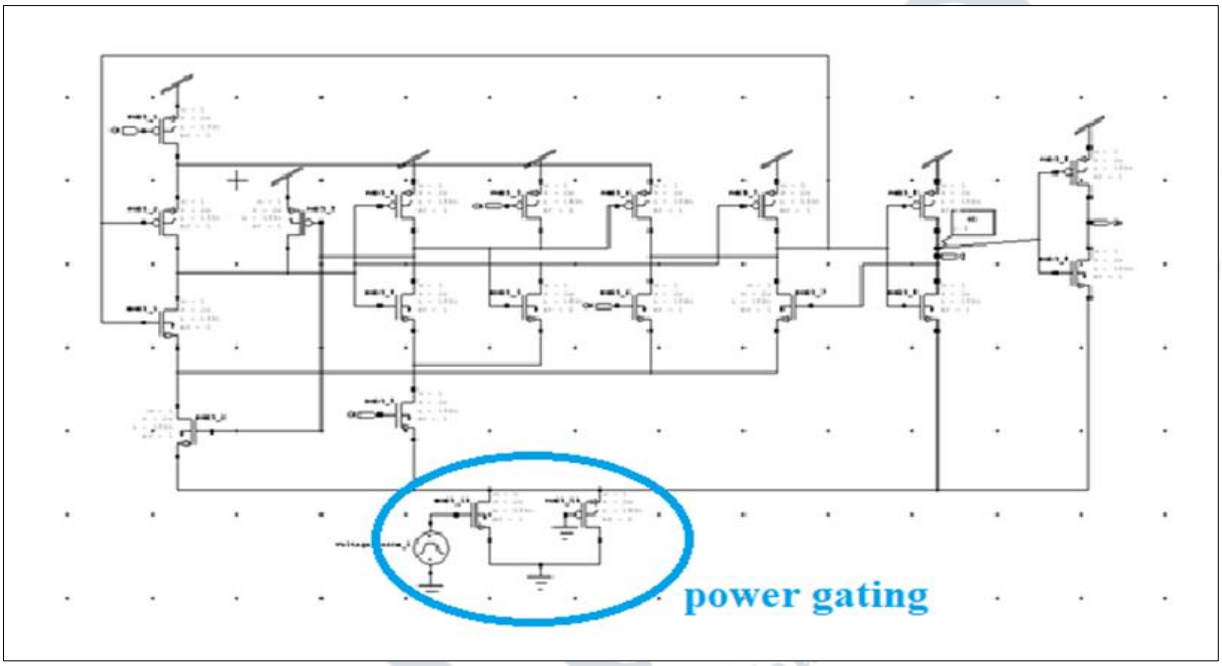

Fig.8: Modified Flip-flop structure using Power Gating

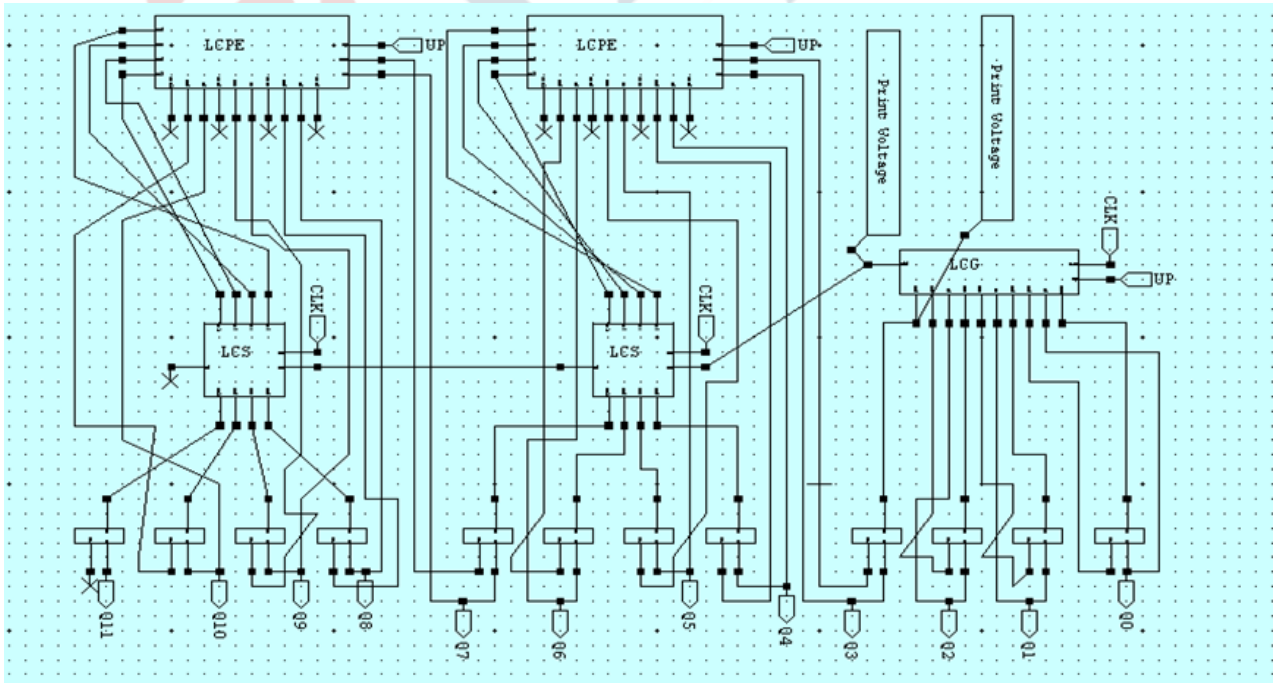

Fig.9: Proposed Counter Architecture

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V. RESULTS & EVALUATION

The Result and Discussion section extensively evaluates the Proposed Counter structure, utilizing S-edit in Tanner EDA. The design underwent rigorous checks to ensure schematic and connection accuracy before simulation using T-Spice. The simulation involved integrating a technology file, defining parameters, specifying input supplies, and executing power and delay calculations. Following simulation, waveform analysis examined MOSFET usage, power consumption, and delay values, providing insights into the structure's behavior and performance indicators. The assessment of MOSFET utilization highlighted efficiency in resource usage, while power analysis evaluated energy efficiency. Additionally, delay analysis offered insights into operational speed.

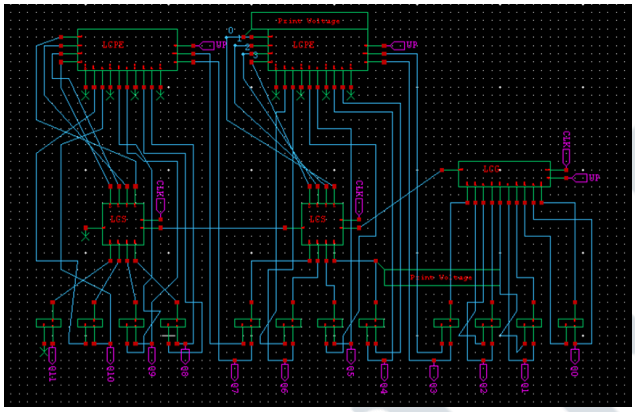

Fig.10: Schematic of proposed counter in Tanner

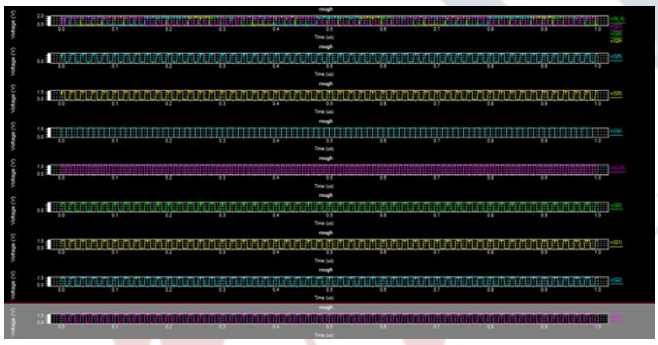

Fig.11: Waveform view of proposed counter

Comparison Table:

Parameters	Power	Delay	Area
Existing	7.706mW	0.739ns	471
Proposed	4.825mW	0.87ns	495

The comparison table offers a detailed breakdown of essential parameters for both the Existing and Proposed designs, without revealing specific numerical data. It encompasses Power, which represents the total power consumption in milliwatts, offering insights into the energy efficiency of each design. Delay, quantified in nanoseconds, shows the speed of the designs, highlighting their information processing rates. Additionally, the Area parameter, expressed in unspecified units, represents the physical dimensions or size of the designs, providing insights into their compactness or complexity. This summary, devoid of numerical data, enables readers to understand the comparative performance aspects without needing specific quantitative information.

VI. CONCLUSION

In summary, this study successfully introduces and implements a synchronous up/down counter in CMOS technology, featuring a mechanism for high-speed local clock generation using gate driver logic. The designed counter provides flexibility for efficient and reliable counting operations, supporting both upward and downward counting modes. The incorporation of gate driver logic for Flip-flop in generating the local clock has been crucial in achieving enhanced speed, thereby enhancing overall performance. The design methodology, emphasizing high-speed local clock generation, introduces a novel approach to the development of synchronous counters in CMOS technology. The research offers valuable insights into innovative methods for achieving rapid counting operations, addressing the evolving needs of modern digital systems.

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